IN THE CLAIMS

Claims 1, 10 and 11 are amended, and claims 5 and 15 are cancelled:

1.   (Currently amended)   A discontinuous transmission (DTX) bit
processing method for a multirate modulation scheme comprising:

    receiving a symbol;

    determining whether the symbol comprises at least one DTX bit;

    mapping the symbol to a predetermined mapping point (S) on an IQ plane,
wherein the symbol is mapped to a signal point in which bits are identical with the
bits consisting of the symbol on the IQ plane, when the symbol has no DTX bits;

    minimizing a transmission power level if the symbol has at least one DTX
bit; and

    transmitting the symbol in the transmission power level of the mapping
point.

2.   (Original)   The method of claim 1, wherein the mapping point is
calculated by averaging signal points in which bits corresponding to non-DTX bits
of the symbol are approximately identical with each other on the IQ plane.

3.   (Original)   The method of claim 2, wherein the mapping point is set in
consideration of at least one of a number of the non-DTX bits, a number of the
selected signal points, and locations of the selected signal points on the IQ
plane.

4.   (Original)   The method of claim 1, wherein the symbol is mapped to an
origin of the IQ plane, when at least one bit of the symbol is a DTX bit.

5.   (Cancelled)

6.   (Original)   The method of claim 2, wherein the mapping point is set in
consideration of plus and minus symbols of the signal points on the IQ plane.

7. (Original) The method of claim 6, wherein the mapping point is set in consideration of at least one of number of the non-DTX bits, number of the selected signal points, and locations of the selected signal points on the IQ plane.

8. (Original) The method of claim 7, wherein the symbol is mapped to an origin of the IQ Plane, when at least one bit of the symbol is a DTX bit.

9. (Original) The method of claim 8, wherein the symbol is mapped to a signal point in which bits are approximately identical with bits comprising the symbol in the IQ plane, if the symbol has no DTX bit.

10. (Currently amended) A transmitter of a base station modem comprising:

a transport channel (TrCH) multiplexer for multiplexing radio frames from a plurality of transport channels into a composite transport channel (CCTrCH);

a discontinuous transmission (DTX) insertion module for inserting DTX bits into the radio frames of the CCTrCH, wherein a symbol is mapped to a signal point in which bits are identical with the bits consisting of the symbol on an IQ plane, when the symbol has no DTX bits;

a physical channel segmentation module for segmenting the CCTrCH for different physical channels (PhCHs) to produce a plurality of segments;

an interleaver for interleaving the segments; and

a physical channel mapping module for mapping the segments to the corresponding PhCHs.

11.   (Currently amended)   A discontinuous transmission (DTX) bit
processing system comprising:

    means for receiving a symbol;

    means for determining whether the symbol comprises at least one DTX
bit;

    means for mapping the symbol to a predetermined mapping point (S) on
an IQ plane, wherein the symbol is mapped to a signal point in which bits are
identical with the bits consisting of the symbol on the IQ plane, when the symbol
has no DTX bits;

    means for minimizing a transmission power level if the symbol has at least
one DTX bit; and

    means for transmitting the symbol in the transmission power level of the
mapping point.

12.   (Original)   The system of claim 11, wherein the mapping point is
calculated by averaging signal points in which bits corresponding to non-DTX bits
of the symbol are approximately identical with each other on the IQ plane.

13.   (Original)   The system of claim 12, wherein the mapping point is set in
consideration of at least one of a number of the non-DTX bits, a number of the
selected signal points, and locations of the selected signal points on the IQ
plane.

14.   (Original)   The system of claim 11, wherein the symbol is mapped to an
origin of the IQ plane, when at least one bit of the symbol is a DTX bit.

15.   (Cancelled)

16.   (Original)   The system of claim 12, wherein the mapping point is set in
consideration of plus and minus symbols of the signal points on the IQ plane.

17. (Original)   The system of claim 16, wherein the mapping point is set in consideration of at least one of number of the non-DTX bits, number of the selected signal points, and locations of the selected signal points on the IQ plane.

18. (Original)   The system of claim 17, wherein the symbol is mapped to an origin of the IQ Plane, when at least one bit of the symbol is a DTX bit.

19. (Original)   The system of claim 18, wherein the symbol is mapped to a signal point in which bits are approximately identical with bits comprising the symbol in the IQ plane, if the symbol has no DTX bit.

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